AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated in the following listing of all claims:

Claims 1-10 **(Canceled)**

11. (Original) A circuit comprising:

a first signal generation circuit for generating an output signal having a frequency which is proportional to that of an input signal, said first signal generation circuit comprising

a first phase locked loop (PLL) circuit for generating an intermediate signal having a frequency which is proportional to the input signal frequency; and

a second phase locked loop circuit for generating the output signal having a frequency which is proportional to the intermediate signal frequency;

wherein, for a given input signal frequency and a given output signal frequency, the intermediate signal frequency is selectable from a plurality of available frequencies.

12. (Original) The circuit of claim 11 wherein the first PLL has a lower bandwidth than the second PLL.

13. (Original) The circuit of claim 11 wherein the input signal is derived from a reference signal for a serial data signal.

14. (Original) The circuit of claim 12 wherein the bandwidth of the first PLL is selectable from a plurality of values.

15. (Original) The circuit of claim 11 wherein the output signal frequency is equal to M times the input signal frequency, where M is a positive integer.

16. (Original) The circuit of claim 11 wherein the output signal frequency is equal to M/N times the input signal frequency, where M and N are both positive integers.

17. (Original) The circuit of claim 11 wherein the output signal frequency is other than an integer ratio times the input signal frequency.

18. (Original) The circuit of claim 11 wherein each of the plurality of available frequencies falls by at least a predetermined offset from any harmonic frequency of the given input signal frequency and the given output signal frequency.

19. (Original) The circuit of claim 18 wherein the plurality of available frequencies numbers at least five.

20. (Original) The circuit of claim 18 wherein the plurality of available frequencies are spaced approximately 2.5% apart, relative to a nominal intermediate signal frequency.

21. (Original) The circuit of claim 18 wherein the plurality of available frequencies are spaced approximately 1.25% apart, relative to a nominal intermediate signal frequency.

22. (Original) The circuit of claim 11 encoded in a computer readable medium suitable for design, test, or manufacture of an integrated circuit.

23. (Original) The circuit of claim 11 further comprising:

a second signal generation circuit for generating a second output signal having a frequency which is proportional to that of a second input signal, said second signal generation circuit comprising

a third phase locked loop (PLL) circuit for generating a second intermediate signal having a frequency which is proportional to the second input signal frequency; and

a fourth phase locked loop circuit for generating the second output signal having a frequency which is proportional to the second intermediate signal frequency;

wherein, for a given second input signal frequency and a given second output signal frequency, the second intermediate signal frequency is selectable from a second plurality of available frequencies.

24. (Original) The circuit of claim 23 wherein the first and second signal generation circuits are substantially identical.

25. (Original) The circuit of claim 23 wherein the first and second signal generation circuits are disposed within a single integrated circuit.

26. (Original) The circuit of claim 23 wherein the first and second signal generation circuits are disposed within different integrated circuits on a single printed wiring board.

27. (Original) The circuit of claim 23 wherein the first and second signal generation circuits are disposed on different printed wiring boards within one system enclosure.

28. (Original) The circuit of claim 23 wherein the first and second input signals are nominally identical in frequency, but associated with independent serial data channels.

29. (Original) The circuit of claim 28 wherein the first mentioned intermediate signal and the second intermediate signal are chosen to have different frequencies.

Claims 30-32 **(Canceled)**

33. (Original) A method comprising:

generating a first intermediate signal having a frequency which is a first factor times a first input signal frequency;

generating a first output signal having a frequency which is a second factor times the first intermediate signal frequency;

choosing the first intermediate signal frequency from a plurality of available frequencies by appropriately choosing the first factor; and

choosing the second factor to result in a desired proportionality between the first input signal and the first output signal.

34. (Original) The method of claim 33 further comprising using a first phase-locked loop circuit to generate the first intermediate signal.

35. (Original) The method of claim 33 further comprising using a second phase-locked loop circuit to generate the first output signal.

36. (Original) The method of claim 35 further comprising configuring the first phase-locked loop circuit with a lower bandwidth than the second phase-locked loop circuit.

37. (Original) The method of claim 33 further comprising choosing the first intermediate signal frequency to avoid harmonics of the first input signal and the first output signal.

38. (Original) The method of claim 33 further comprising:

generating a second intermediate signal having a frequency which is a third factor times a second input signal frequency;

generating a second output signal having a frequency which is a fourth factor times the second intermediate signal frequency;

choosing the second intermediate signal frequency from a second plurality of available frequencies by appropriately choosing the third factor; and

choosing the fourth factor to result in a desired proportionality between the second input signal and the second output signal.

39. (Original) The method of claim 38 further comprising generating the first and second output signals within a single integrated circuit.

40. (Original) The method of claim 38 further comprising generating the first and second output signals on a single printed wiring board.

41. (Original) The method of claim 38 further comprising generating the first and second output signals on different printed wiring boards within one system enclosure.

42. (Original) The method of claim 38 wherein the first and second intermediate frequencies are chosen to be different frequencies.

43. (New) The circuit of claim 23 wherein the first and second signal generation circuits each comprises a clock multiplying circuit.

44. (New) The circuit of claim 43 wherein the first and second signal generation circuits each comprises a portion of a serial digital communications circuit.